SIS8300
µTCA FOR PHYSICS Digitizer

User Manual

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Revision Table:

Revision	Date	Modification
0.01	21.06.10	Based on AG notes
0.02	18.08.10	Clock Distribution
0.03	25.08.10	Vendor Id./PCI Id.
0.04	27.08.10	Register inlays
0.05	17.09.10	Add registers
0.06	18.09.10	Front panel description
0.07	06.10.10	RTM connectors
1.00	08.10.10	DAC comment
1.01	22.10.10	V0103 Firmware Release
1.02	19.10.10	JTAG over PCIe Index entry
1.03	17.03.11	JTAG parallel load note
2.00	28.06.11	Changes with new PCB version V2 - changed DAC interface - add FPGA CRC check register RTM management chapter

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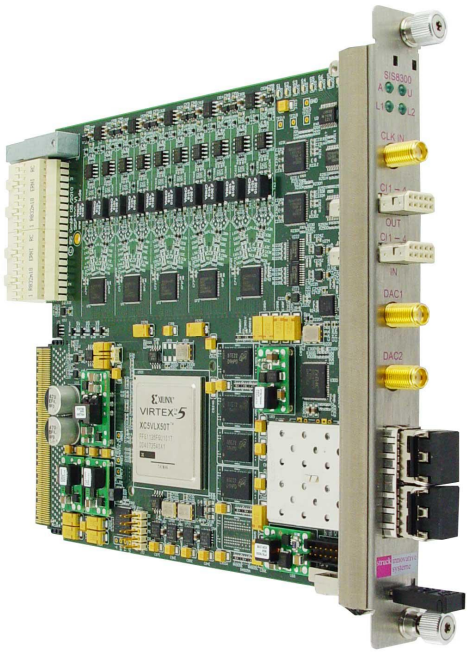
1 Introduction

The SIS8300 is a ten 10 channel 125 MS/s digitizer with 16-bit resolution according to the uTCA for Physics draft standard.



SIS8300 with SFPs installed

As we are aware, that no manual is perfect, we appreciate your feedback and will incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.html .

Note 1: It is PICMG's policy to prohibit claims of compliance with respect to a specification under development. Any such claims must be understood as applying to a draft, which is subject to change

Note 2: The SIS8300 is developed in co-operation with DESY under ZIM grant 2460101MS9
(ZIM: Zentrales Innovationsprogramm Mittelstand)

1.1 Related documents

A list of available firmware designs can be retrieved from http://www.struck.de/sis8300firm.html

2 Design

The central building block of the SIS8300 card is a Xilinx Virtex 5 FPGA. It holds the 4 lane PCI Express interface and is in control of all active components.

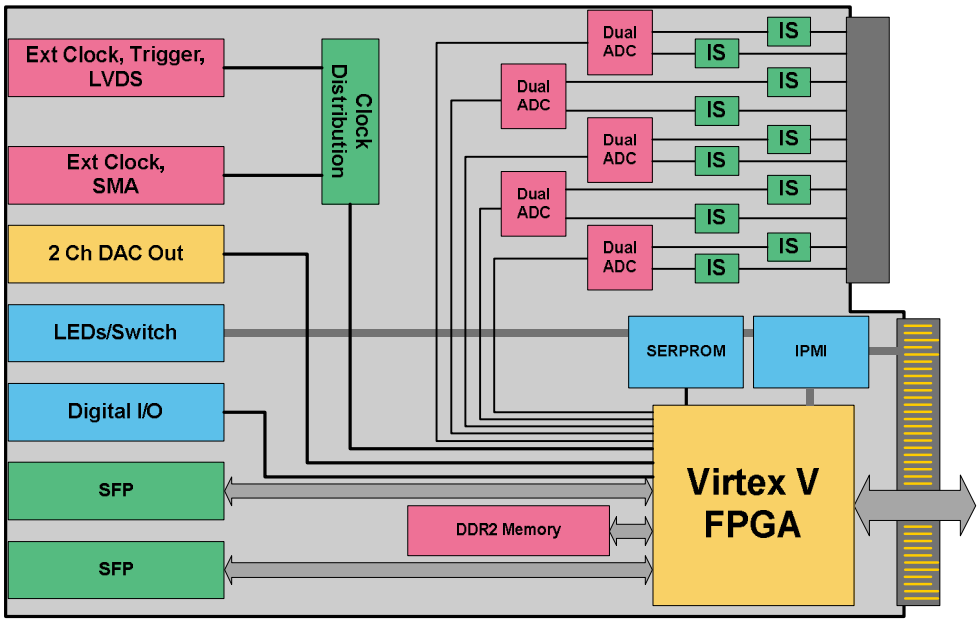
2.1 Functionality

The key properties of the SIS8300 card are listed below.

- Double size µTCA for Physics Board
- 4 Lane PCI Express Interface
- Dual SFP Card Cage for optional Multi Gigabit Link
- Xilinx Virtex 5 FPGA
- DDR2 Memory Interface
- 4 x 1 GBit default DDR2 memory
- Atmega128 IPMI
- External Clock and Trigger Inputs
- Frontpanel digital I/O (4in/4 out) on Harlink Connectors
- RTM ADC Analog Inputs, I2C-Bus
- 10 ADC Channels 125MS/s, 16-Bit
- 2 DAC Channels 250MS/s, 16-Bit
- Clock distribution with phase shifting
- 4 M-LVDS µTCA Ports
- 2 µTCA Clocks

2.2 Block Diagram

A simplified block diagram of the SIS8300 is shown below.

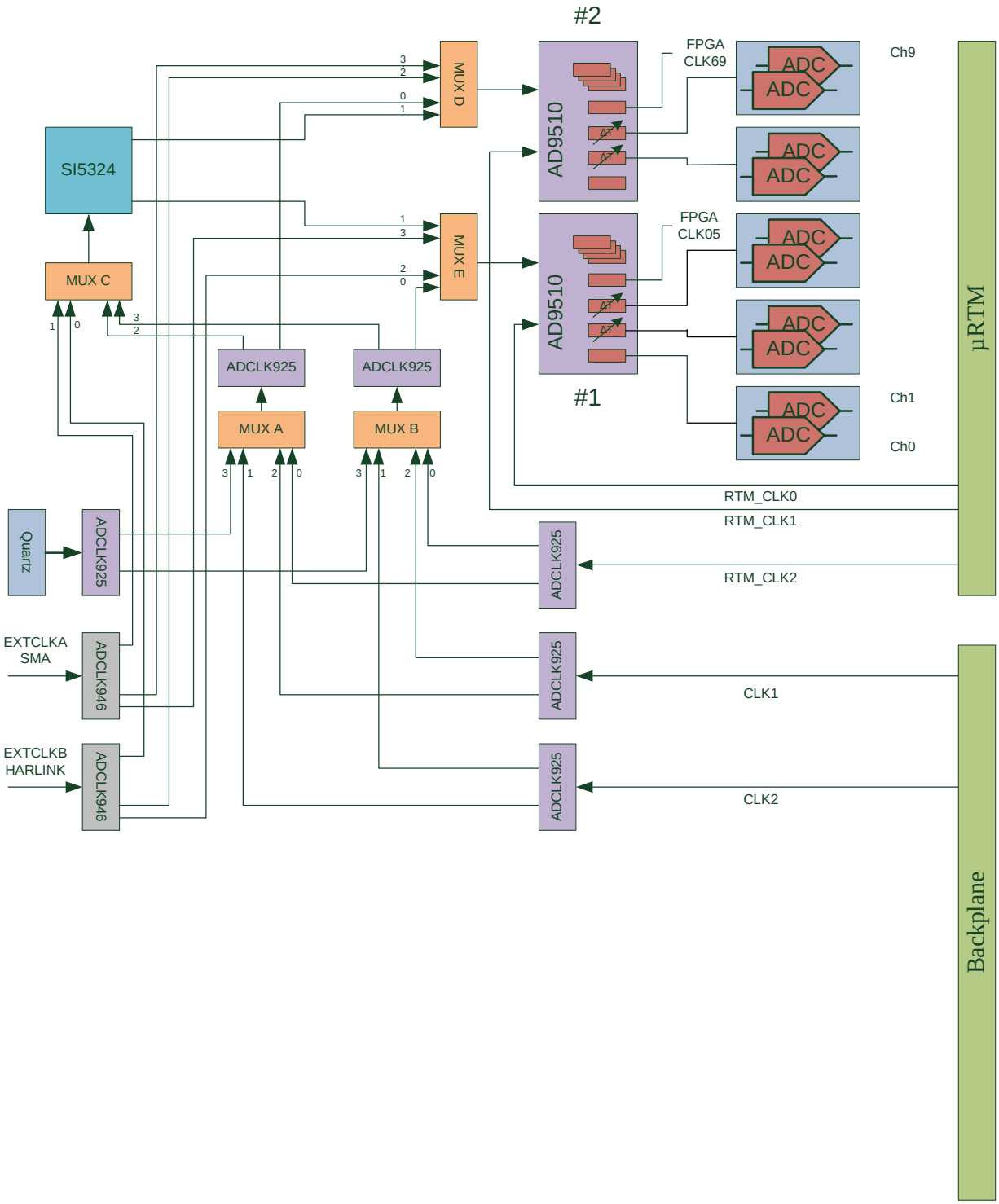


2.3 Platform Management

The management code of the SIS8300 is implemented in an Atmel Atmega1281-16MU microcontroller and can be upgrade in field over connector J32 (see section 3.3).

2.4 Clock Distribution

The clock distribution scheme of the SIS8300 is illustrated below.

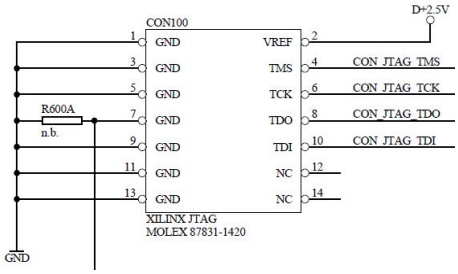


3 Jumper/Connector Pin Assignments

The following subsections describe the pin assignments of jumpers and connectors.

3.1 CON100 JTAG

The SIS8300's on board logic can load its firmware from a serial PROM, via the JTAG port on connector CON100, PCI Express or via the MMC.
Hardware like the XILINX HW-USB-JTAG in connection with the appropriate software will be required for in field JTAG firmware upgrades.
CON100 is a 2mm (i.e. metric) 14 pin header that allows you to reprogram the firmware of the SIS8300 board with a JTAG programmer. The pin out is shown in the schematic below. It is compatible with the cable that comes with the XILINX HW-USB-II-G-JTAG platform cable. CON100 can be found at the right bottom side of the board.



Note 1: The board has to be powered for reprogramming over JTAG

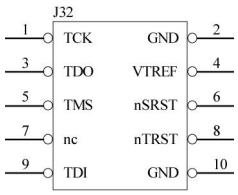
Note 2: The FPGA uses 8-bit parallel mode to load the firmware from the serial PROM. Make sure to check the 'Parallel Load' box in Impact when specifying the programming properties for the PROM.

3.2 J604 Watchdog Reset

J604 can be found next to the left upper edge of U500 (largest chip on the card). With J604 closed the boards watchdog reset is connected to the reset logic. J604 should be opened for JTAG firmware programming.

3.3 J32 AVR JTAG

This 10-pin header is used to connect to the JTAG of the Atmel Atmega128 microcontroller providing the IPMI/MCH functionality of the SIS8300.



4 LEDs

4.1 AMC LEDs

The AMC LEDs are implemented according to the standard.

4.2 Front Panel LEDs

The SIS8300 in Gigalink stuffing option has 4 green front panel LEDs.

LED name	Function in Gigalink design
A	PCI Express Access
U	User LED
L1	PCIe Link up (Optical Link 1 up)
L2	ADC Sampling active (Optical Link 2 up)

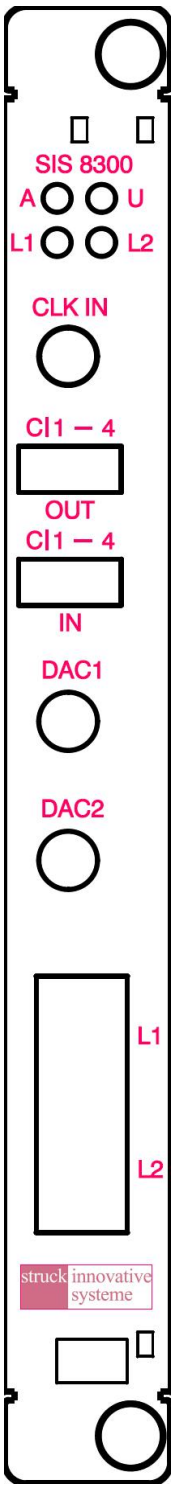
4.3 SMD LEDs

A number of surface mount red LEDs are on the SIS8300 to visualize part of the board status.

LED designator	LED comment	Function
D20A	S1	Firmware dependent
D20B	S2	Firmware dependent
D20C	S3	Firmware dependent
D20D	S4	Firmware dependent
D20E	S5	Firmware dependent
D20F	S6	Firmware dependent
D20G	S7	Firmware dependent
D20H	S8	Firmware dependent
D21D	READY	FPGA ready
D105A	TX FAULT 1	Link 1 transmitter fault
D105B	RX LOS 1	Link 1 receiver loss of signal
D110A	TX FAULT 2	Link 2 transmitter fault
D110B	RX LOS 2	Link 2 receiver loss of signal

5 Front panel

The SIS8300 is a µTCA for Physics board. A sketch of the front panel is shown below.



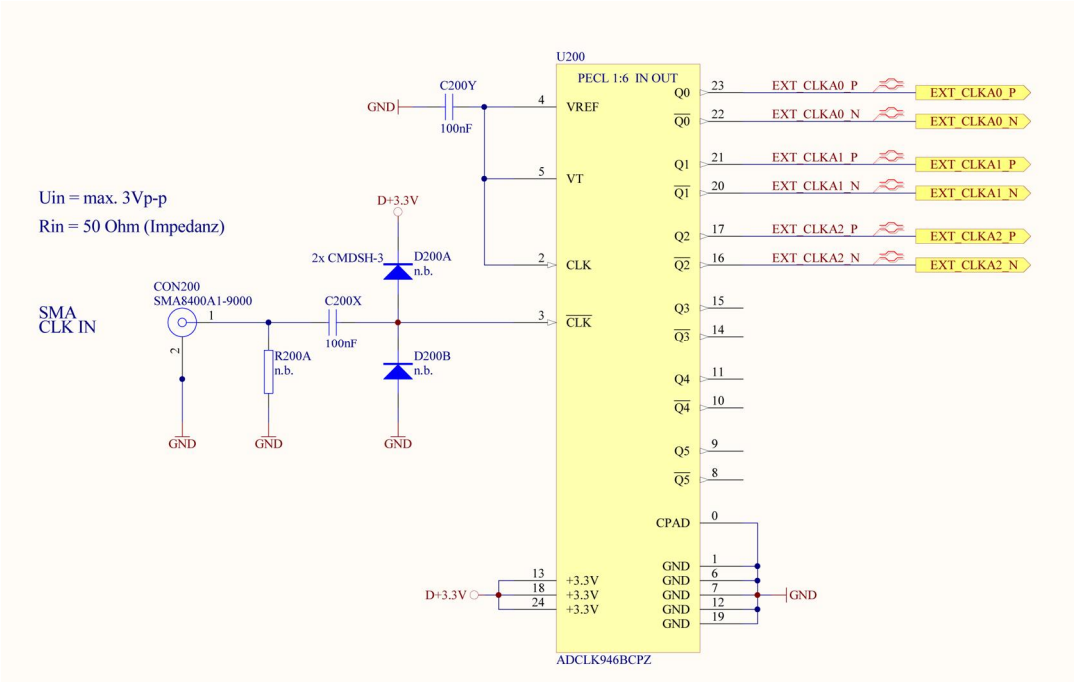
5.1 Harlink LVDS In-/Outputs

The Harlink LVDS Output and Input connectors have 5 signals each. The Clock signal to the left hand side is marked with C and the other 4 signals are labelled with 1-4.

	Clock	1	2	3	4
Top	P	P	P	P	P
Bottom	N	N	N	N	N

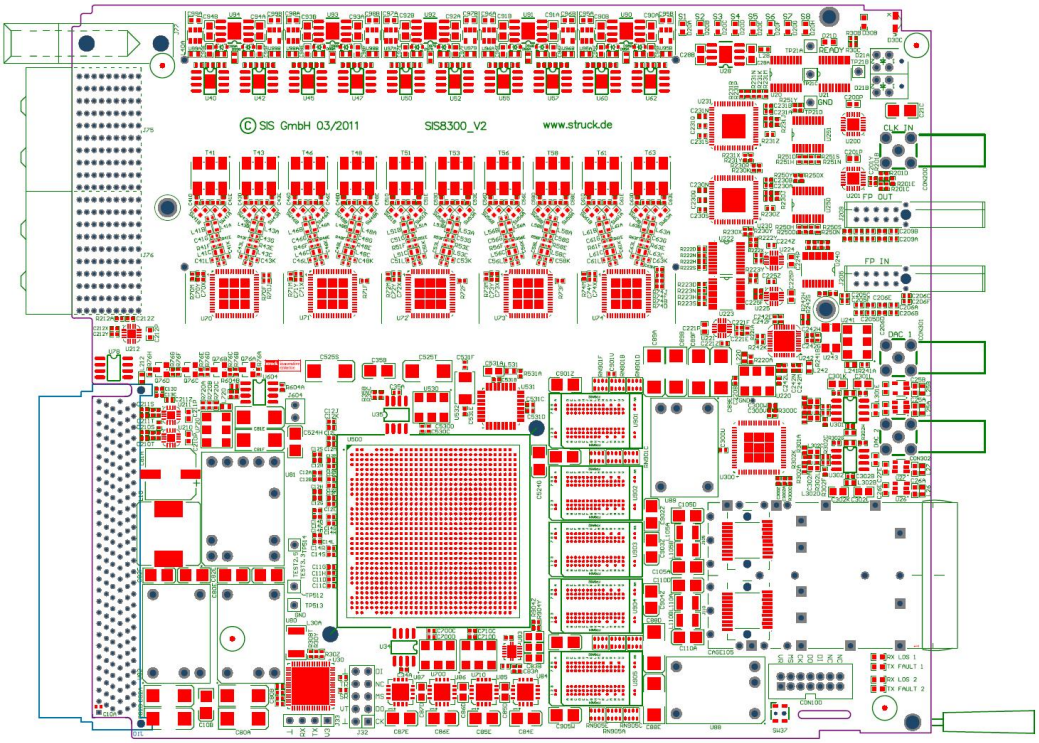
5.2 SMA Clock Input

The front panel SMA clock input is designed to accept a maximum peak to peak signal level of 3V into 50 Ohms. The clock input signal is coupled to the internal logic via a capacitor. The schematic of the input stage is shown below.



6 Board Layout

A print of the silk screen of the component side is shown below.



Connector types
The used connectors are listed in the table below.

Designator	Function	Manufacturer	Part Number
CON100	JTAG	Molex	87831-1420
CON200	Clock In	JYEBAO	SMA8400A1-9000
CON301	DAC 1 Out	JYEBAO	SMA8400A1-9000
CON302	DAC 2 Out	JYEBAO	SMA8400A1-9000
CAGE105	SFP Cage, 2 Ports	TYCO	1761014-1
J10	AdvancedMC	HARTING	16211701301000
J32	JTAG Atmega	SAMTEC	HTSW-105-26-G-D
J75	RTM	ERNI	ERmetZD-10x3P-FEM
J76	RTM	ERNI	ERmetZD-10x3P-FEM
J77	RTM Keying	TYCO	(*)
J209	Trigger & Clock Out	HARTING	27 21 121 8000
J205	Trigger & Clock In	HARTING	27 21 121 8000
J604	Watchdog	SAMTEC	HTSW-102-26-G-S

Note (*): The used Key may depend on the hardware configuration of the SIS8300

7 Firmware Description

7.1 Address Map

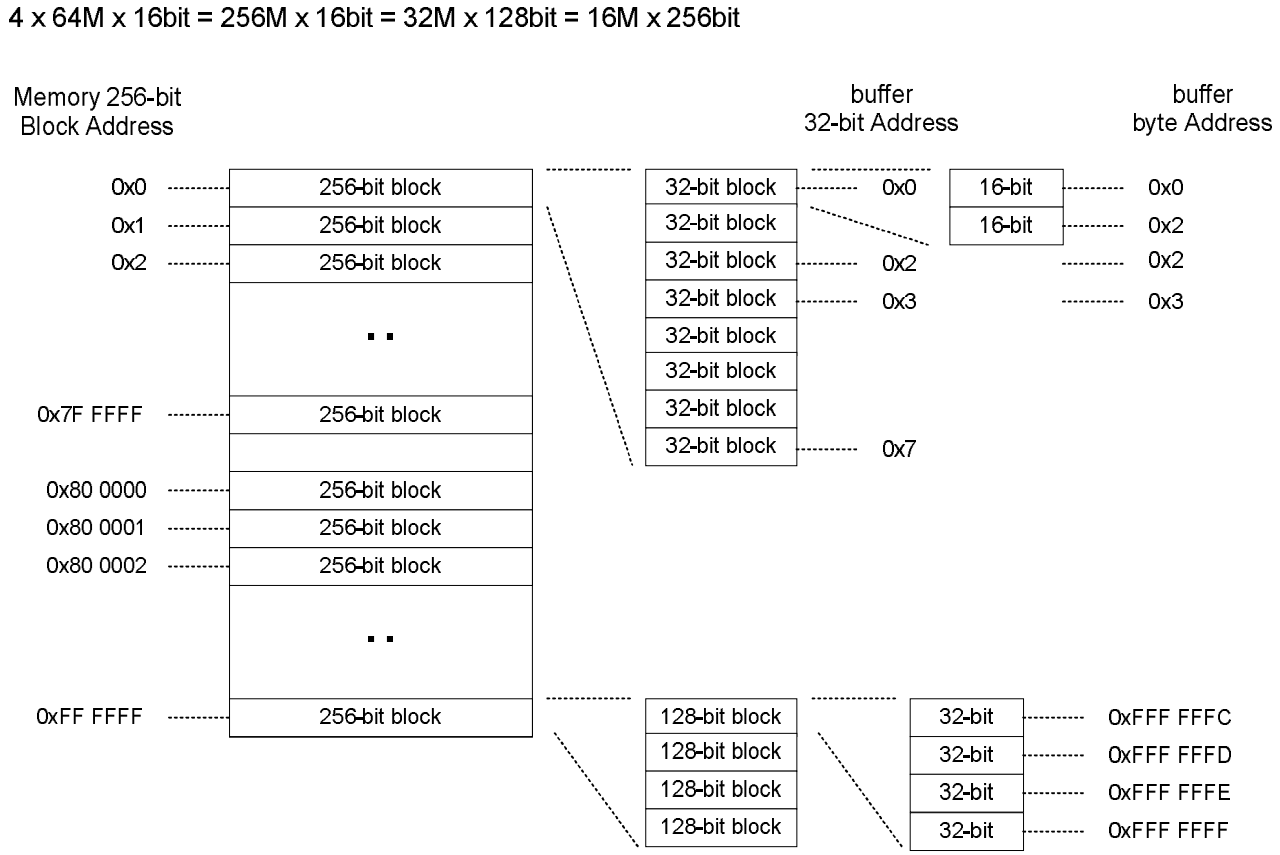
Following 32-bit addresses are implemented

Offset	Access	Function
0x000	R	Module Identifier/Firmware Version register
0x001	R	Serial number register
0x002	R/W	XILINX JTAG register
0x003	R	XILINX Virtex5 configuration memory Error Detection register
0x004	R/W	User Control/Status register (JK)
0x010	R/W	ADC Acquisition Control/Status register
0x011	R/W	ADC Sample Control register
0x012	R/W	MLVDS Input/Output Control register
0x013	R/W	Harlink Connector Input/Output Control register
0x014	R/W	free
0x015	R/W	free
0x016	R/W	free
0x017	R/W	free
0x40	R/W	Clock Distribution Multiplexer control register
0x41	R/W	Clock Distribution IC AD9510 SPI interface register
0x42	R/W	Clock Multiplier IC SI5326 SPI interface register
0x44	R/W	reserved
0x45	R/W	DAC Control register
0x46	R/W	DAC Data register
0x48	R/W	ADC SPI Interface register
0x49	R/W	ADC Input Tap delay register
0x90	R/W	VIRTEX5_SYSTEM_MONITOR_DATA register
0x91	R/W	VIRTEX5_SYSTEM_MONITOR_ADDR register
0x92	R/W	VIRTEX5_SYSTEM_MONITOR_CTRL register
0x100	R/W	ADC ch1 Trigger Setup register
0x101	R/W	ADC ch2 Trigger Setup register
..		
0x109	R/W	ADC ch10 Trigger Setup register
0x110	R/W	ADC ch1 Trigger Threshold register
0x111	R/W	ADC ch2 Trigger Threshold register
..		
0x119	R/W	ADC ch10 Trigger Threshold register

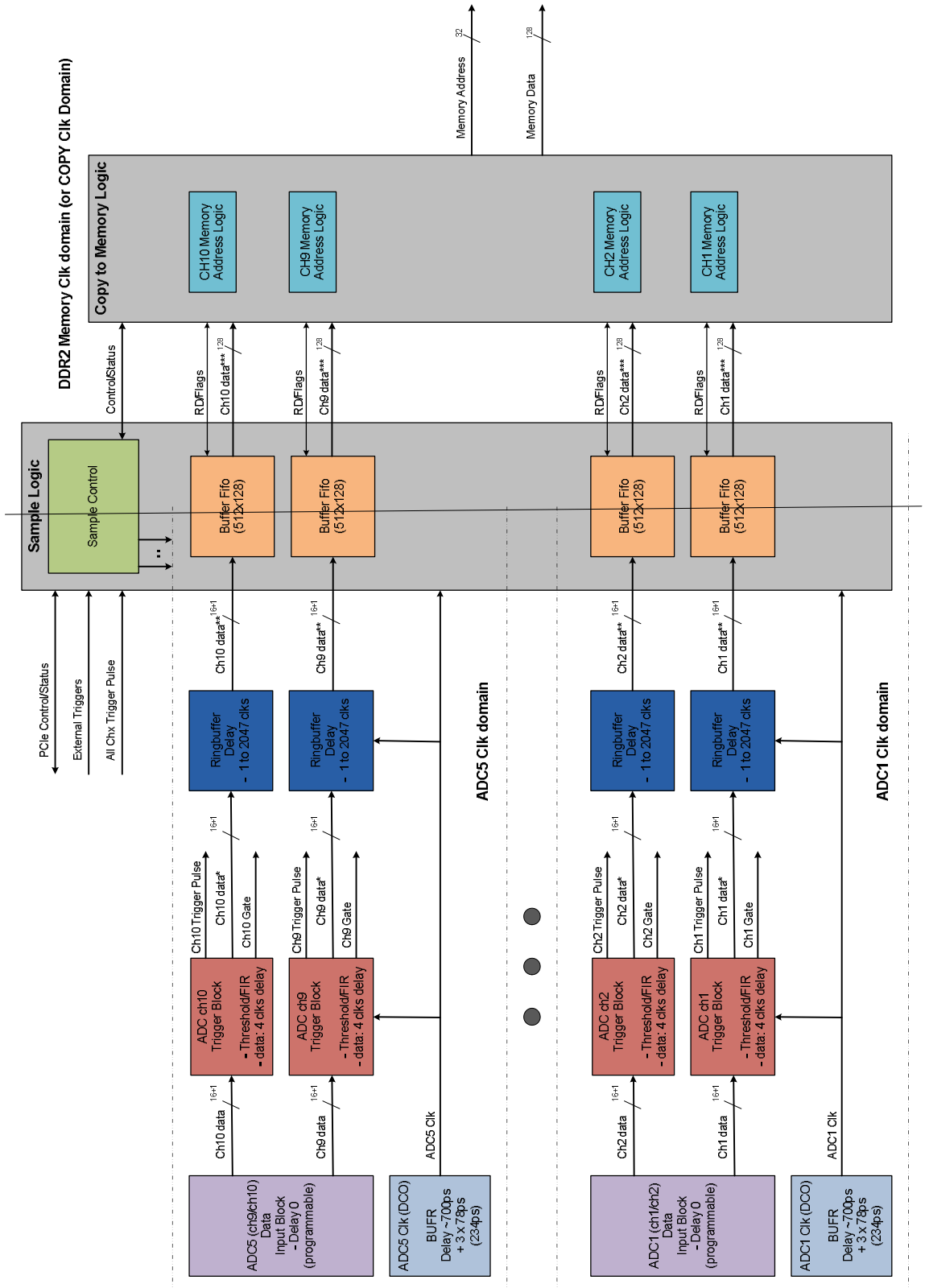
0x120	R/W	ADC ch1 Memory Sample Start Address / Actual Address register
0x121	R/W	ADC ch2 Memory Sample Start Address / Actual Address register
..		
0x129	R/W	ADC ch10 Memory Sample Start Address / Actual Address register
0x12A	R/W	ADC chx Sample Length Register
0x12B	R/W	ADC chx Ringbuffer Pretrigger Delay (0 to 2046)
0x12C	R/W	free
0x12D	R/W	free
0x12E	R/W	free
0x12F	R/W	free
0x200	R/W	DMA_READ_DST_ADR_LO32
0x201	R/W	DMA_READ_DST_ADR_HI32
0x202	R/W	DMA_READ_SRC_ADR_LO32
0x203	R/W	DMA_READ_LEN
0x204	R/W	DMA_READ_CTRL
	R/W	
0x210	R/W	DMA_WRITE_SRC_ADR_LO32
0x211	R/W	DMA_WRITE_SRC_ADR_HI32
0x212	R/W	DMA_WRITE_DST_ADR_LO32
0x213	R/W	DMA_WRITE_LEN
0x214	R/W	DMA_WRITE_CTRL
	R/W	
0x230	R/W	MEMORY test Mode register
0x211	R/W	DMA_WRITE_SRC_ADR_HI32
	R/W	
	R/W	
	R/W	
	R/W	
	R/W	
0x3ff	W	Bit 0 = 1: Master Reset (reset all registers)

7.2 Memory buffer

The structure of the memory buffer with 512 MByte (i.e. 4 x 1 GBit memory chips) is illustrated below.



7.3 ADC Sample Logic



7.4 Module Id. and Firmware Revision register

#define SIS8300_IDENTIFIER_VERSION_REG 0x00

This register holds the module identifier (SIS8300) and the firmware version and revision.

BIT	access	Name	Function
31-16 FFFF0000	RO	Module Identifier	0x8300
15-8 0000FF00	RO	Firmware Version	1..255
7-0 000000FF	RO	Firmware Revision	1..255

Example: The initial version of the SIS8300 reads 0x83000101

7.5 Serial Number register

#define SIS8300_SERIAL_NUMBER_REG 0x01

This register holds the Serial Number of the module.

BIT	access	Name	Function
31-16 FFFF0000	RO	reserved	
15-0 0000FFFF	RO	Serial Number	1..65535

7.6 XILINX JTAG register

#define SIS8300_XILINX_JTAG_REG 0x02

XILINX JTAG register

This register is used in the firmware upgrade process over PCIe only. A TCK is generated upon a write cycle to this register.

Bit	write Function	read Function
31	none	TDO
30	...	1 x Shifted TDO
...	...	
4	none	
3	none	
2	none	
1	TMS	
0	TDI	30 x Shifted TDO

The read register function operates as a shift register for TDO. The content of the read register is shifted to the right by one bit with every positive edge of TCK and the status of TDO is transferred to Bit 30. Bit 31 reflects the current value of TDO during a read access.

7.7 XILINX Virtex5 Error Detection register

#define SIS8300_XILINX_ECC_REG 0x03

XILINX Virtex5 configuration memory error detection register.

Bit	read Function
31	0
30	0
...	
16	0
15	Frame ECC output indicating a valid SYNDROME value
14	0
13	CRC Error
12	ECC Error
11	SYNDROME: Status bit 11
..	
1	SYNDROME: Status bit 1
0	SYNDROME: Status bit 0

7.8 User Control/Status register

#define SIS8300_USER_CONTROL_STATUS_REG 0x04

The control register is implemented as a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which location is 16-bit higher in the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time. The only function at this point in time is user LED on/off.
On read access the same register represents the status register.

Bit	write Function	read Function
31	Clear reserved 15 (*)	0
30	Clear reserved 14 (*)	0
29	Clear reserved 13 (*)	0
28	Clear reserved 12 (*)	0
27	Clear reserved 11 (*)	0
26	Clear reserved 10 (*)	0
25	Clear reserved 9 (*)	0
24	Clear reserved 8 (*)	0
23	Clear reserved 7 (*)	0
22	Clear reserved 6 (*)	0
21	Clear reserved 5 (*)	0
20	Clear reserved 4 (*)	0
19	Clear reserved 3 (*)	0
18	Clear reserved 2 (*)	0
17	Clear reserved 1 (*)	0
16	Switch off user LED (*)	0
15	Set reserved 15	Status reserved 15
14	Set reserved 14	Status reserved 14
13	Set reserved 13	Status reserved 13
12	Set reserved 12	Status reserved 12
11	Set reserved 11	Status reserved 11
10	Set reserved 10	Status reserved 10
9	Set reserved 9	Status reserved 9
8	Set reserved 8	Status reserved 8
7	Set reserved 7	Status reserved 7
6	Set reserved 6	Status reserved 6
5	Set reserved 5	Status reserved 5
4	Set reserved 4	Status reserved 4
3	Set reserved 3	Status reserved 3
2	Set reserved 2	Status reserved 2
1	Set reserved 1	Status reserved 1
0	Switch on user LED	Status User LED (1=LED on, 0=LED off)

(*) denotes power up default setting

7.9 ADC Acquisition Control/Status register

```
#define SIS8300_ACQUISITION_CONTROL_STATUS_REG       0x10  /* rd/wr D32 */
```

Bit	write	read
31		
30		
29		
28		
...		
...		
17		
16		
15		
12		
11		
10		
9		
8		
7		Status: DDR2 Memory OK
6		
5		Status: internal Sample Buffer Not Empty
4		Status: internal Sample Logic Busy
3		
2	'1' : Disable Sampling (Reset Sample Logic)	
1	'1' : Arm Sampling (Start with next trigger)	Status: Arm for trigger (Wait for trigger)
0	'1' : Start Sampling immediately (Arm and Start/Trigger)	Status: Sampling Busy

The power up default value is 0x0

7.10 ADC Sample Control register

```
#define SIS8300_SAMPLE_CONTROL_REG       0x11  /* rd/wr D32 */
```

ADC channels can be disabled from storing data to memory by setting the corresponding disable bit in this register.

Bit	write
31	
30	
29	
28	
...	
...	
17	
16	
15	
12	
11	Enable external Trigger
10	Enable internal Trigger
9	Disable Sampling Ch10
8	Disable Sampling Ch9
7	
6	
5	
4	
3	
2	Disable Sampling Ch3
1	Disable Sampling Ch2
0	Disable Sampling Ch1

The power up default value is 0x0

7.11 MLVDS Input/Output Control register

```
#define SIS8300_MLVDS_IO_CONTROL_REG     0x12  /* rd/wr D32 */
```

Bit	Write	Read
31	Enable LVDS Output Bit 7	Enable LVDS Output Bit 7
30	Enable LVDS Output Bit 6	Enable LVDS Output Bit 6
..		
25	Enable LVDS Output Bit 1	Enable LVDS Output Bit 1
24	Enable LVDS Output Bit 0	Enable LVDS Output Bit 0
23	LVDS Output Bit 7	LVDS Output Bit 7
22	LVDS Output Bit 6	LVDS Output Bit 6
...		
17	LVDS Output Bit 1	LVDS Output Bit 1
16	LVDS Output Bit 0	LVDS Output Bit 0
15	LVDS Input 7 External Trigger Enable	LVDS Input 7 External Trigger Enable
14	LVDS Input 6 External Trigger Enable	LVDS Input 6 External Trigger Enable
...		
9	LVDS Input 1 External Trigger Enable	LVDS Input 1 External Trigger Enable
8	LVDS Input 0 External Trigger Enable	LVDS Input 0 External Trigger Enable
7	LVDS Input 7 External Trigger falling edge	LVDS Input Bit 7
6	LVDS Input 6 External Trigger falling edge	LVDS Input Bit 6
...		
1	LVDS Input 1 External Trigger falling edge	LVDS Input Bit 1
0	LVDS Input 0 External Trigger falling edge	LVDS Input Bit 0

Note: external trigger in signals are synchronized with the FPGA CLK05

7.12 Harlink Connector Input/Output Control register

```
#define SIS8300_HARLINK_IO_CONTROL_REG   0x13  /* rd/wr D32 */
```

Bit	Write	Read
31	No function	0
30	No function	0
..		
21	No function	0
20	No function	0
19	Harlink Output 4	Harlink Output 4
18	Harlink Output 3	Harlink Output 3
17	Harlink Output 2	Harlink Output 2
16	No function	0
15	Harlink Input 4 External Trigger falling edge	Harlink Input 4 External Trigger falling edge
14	Harlink Input 3 External Trigger falling edge	Harlink Input 3 External Trigger falling edge
13	Harlink Input 2 External Trigger falling edge	Harlink Input 2 External Trigger falling edge
12	Harlink Input 1 External Trigger falling edge	Harlink Input 1 External Trigger falling edge
11	Harlink Input 4 External Trigger Enable	Harlink Input 4 External Trigger Enable
10	Harlink Input 3 External Trigger Enable	Harlink Input 3 External Trigger Enable
9	Harlink Input 2 External Trigger Enable	Harlink Input 2 External Trigger Enable
8	Harlink Input 1 External Trigger Enable	Harlink Input 1 External Trigger Enable
7	No function	0
6	No function	0
5	No function	0
4	No function	0
3	No function	Harlink Input 4
2	No function	Harlink Input 3
1	No function	Harlink Input 2
0	No function	Harlink Input 1

Harlink Connector Input(1) : external trigger In
Harlink Connector Output(1) : adc chx (or) trigger out

Note: external trigger in signals are synchronized with the FPGA CLK05

7.13 Clock Distribution Multiplexer control register

#define SIS8300_CLOCK_DISTRIBUTION_MUX_REG 0x40

The SIS8300 has 5 IDT ICS853S057 clock multiplexer chips, which are labelled A to E in the clock distribution schematic in section 2.4. The multiplexer control register holds the two select bits for the 5 multiplexer chips as shown in the table below.
The assignment of the inputs to the resources (i.e. clock inputs) is listed in subsection 7.13.1.

BIT	access	Name	Function
31-12 FFFFF000	R/W	reserved	no
11-10 00000C00	R/W	MUXE_SEL	Multiplexer E select bits
9-8 00000300	R/W	MUXD_SEL	Multiplexer D select bits
7-6 000000C0	R/W	reserved	no
5-4 00000030	R/W	MUXC_SEL	Multiplexer C select bits
3-2 0000000C	R/W	MUXB_SEL	Multiplexer B select bits
1-0 00000003	R/W	MUXA_SEL	Multiplexer A select bits

7.13.1 Clock Multiplexer input signal assignments

7.13.1.1 Multiplexer A Input Signals:

U222 - Sel0 and Sel1 (MUX1A_SEL) = Multiplexer A select lines

Sel1	Sel0	Selected Input - Net Name	Clock source Description
0	0	RTMCLK_0	Clock 2 from µRTM card
0	1	TCLKB_0	Clock 2 (Telecom Clock B) from AMC Connector (Backplane)
1	0	TCLKA_0	Clock 1 (Telecom Clock A) from AMC Connector (Backplane)
1	1	OSC_CLK0	Onboard Clock chip (250MHz)

7.13.1.2 Multiplexer B Input Signals:

U223 - Sel0 and Sel1 (MUX1B_SEL) = Multiplexer B select lines

Sel1	Sel0	Selected Input - Net Name	Clock source Description
0	0	RTMCLK_1	Clock 2 from µRTM card
0	1	TCLKB_1	Clock 2 (Telecom Clock B) from AMC Connector (Backplane)
1	0	TCLKA_1	Clock 1 (Telecom Clock A) from AMC Connector (Backplane)
1	1	OSC_CLK1	Onboard Clock chip (250MHz)

7.13.1.3 Multiplexer C Input Signals:

U240 - Sel0 and Sel1 (MUXAB_SEL) = Multiplexer C select lines

Sel1	Sel0	Selected Input - Net Name	Clock source Description
0	0	EXT_CLKB0	Clock from Harlink Connector “CI1-4 IN” (frontpanel)
0	1	EXT_CLKA0	Clock from SMA Connector “CLK IN” (frontpanel)
1	0	MUXA_CLK1	Multiplexer A Output Signal
1	1	MUXB_CLK1	Multiplexer B Output Signal

7.13.1.4 Multiplexer D Input Signals:

U250 - Sel0 and Sel1 (MUX2A_SEL) = Multiplexer D select lines

Sel1	Sel0	Selected Input - Net Name	Clock source Description
0	0	MUXA_CLK0	Multiplexer A Output Signal
0	1	MUL_CLK1	Clock Multiplier (U242) Output 2 Signal
1	0	EXT_CLKB1	Clock from Harlink Connector “CI1-4 IN” (frontpanel)
1	1	EXT_CLKA1	Clock from SMA Connector “CLK IN” (frontpanel)

7.13.1.5 Multiplexer E Input Signals:

U251 - Sel0 and Sel1 (MUX2B_SEL) = Multiplexer E select lines

Sel1	Sel0	Selected Input - Net Name	Clock source Description
0	0	MUXB_CLK0	Multiplexer B Output Signal
0	1	MUL_CLK0	Clock Multiplier (U242) Output 1 Signal
1	0	EXT_CLKB2	Clock from Harlink Connector “CI1-4 IN” (frontpanel)
1	1	EXT_CLKA2	Clock from SMA Connector “CLK IN” (frontpanel)

7.14 Clock Distribution AD9510 Serial Interface (SPI) interface register (0x41, read/write)

```
#define SIS8300_AD9510_SPI_REG          x41  /* read/write; D32 */
```

The parameters of the Clock Distribution IC AD9510 chips can be configured with the SPI (serial Peripheral Interface).

Bit	Write	read	
31	Cmd Bit 1	Write/Read Logic BUSY Flag	
30	Cmd Bit 0		
29	Set “Function” Output Level	Status of Set “Function” Output Level	
28	Select “Function” synchronisation CLK	Status of Select “Function” synchronisation CLK	
...			
...			
25		Status AD9510 #2	
24	AD9510 #2 Select Bit	Status AD9510 #1	
23	Read Cycle Bit		RW CMD
22			
21			
20	Address Bit 12		
19	Address Bit 11		
12	Address Bit 4		
11	Address Bit 3		
10	Address Bit 2		
9	Address Bit 1		
8	Address Bit 0		
7	Write Data Bit 7 (MSB)	Read Data Bit 7 (MSB)	
6	Write Data Bit 6	Read Data Bit 6	
..			
1	Write Data Bit 1	Read Data Bit 1	
0	Write Data Bit 0 (LSB)	Read Data Bit 0 (LSB)	

The power up default value is 0x20000000

Command Bit (31:30) Explanation:

Cmd Bit 1	Cmd Bit 0	Command
0	0	No Function
0	1	R/W CMD
1	0	Function CMD Generates a pulse at the Function Input pin of the AD9510 which is synchronous to the selected clock. The clock selection is done via Bit 28 (Function Syn CLK). The actual function depends on the programming of the selected AD9510
1	1	Reserved

Select “Function” synchronisation CLK Bit (28) Explanation:

Bit 28	Clock Source
0	PCI Clock
1	FPGA CLK 69

Note:

1. enable READ by writing 0x90 to addr 0x0
2. and set Read Cycle Bit

Note:
Please refer to the SIS8300_AD9510_SPI_Setup routine as illustration and to the AD9510 documentation for details.

7.15 Clock Multiplier IC SI5326 SPI interface register

```
#define SIS8300_CLOCK_MULTIPLIER_SPI_REG       x42 /* rd/wr */
```

Clock Multiplier IC SI5326 SPI interface register

Several parameters of the Clock Multiplier SI5326 chip can be configured with the SPI (serial Peripheral Interface).
Please refer to the documentation of the SI5326chip for details.

Bit	Write	read
31	Cmd Bit 1	Write/Read Logic BUSY Flag
30	Cmd Bit 0	Reset, Decrement or Increment Cmd BUSY Flag
29		
...		
17		Si53xx LOL Status
16		Si53xx INT_C1B Status
15	Instruction Byte Bit 7	
..		
..		
8	Instruction Byte Bit 0	
7	Address/Data Byte Bit 7	Read Data Bit 7 (MSB)
..		
..	..	Read Data Bit 1
0	Address/Data Byte Bit 0	Read Data Bit 0 (LSB)

The power up default value is 0x0

Cmd Bit 1	Cmd Bit 0	Command
0	0	Execute SPI Write/Read Cmd
0	1	Reset Cmd
1	0	Decrement Cmd
1	1	Increment Cmd

Reset Cmd: generates an 1us reset pulse

Decrement Cmd: generates an 1us Skew Decrement pulse
Increment Cmd: generates an 1us Skew Increment pulse

Note: INC/DEC Time between consecutive pulses must be greater than 16ms !

7.16 DAC Control register (0x45, read/write)

```
#define SIS8300_DAC_CONTROL_REG     0x45  /* read/write; D32 */
```

Bit	write	read
31		
...		
16		
15		
…		
12		
11		
10		
9		
8	DAC DCM Reset pulse	
7		
6		
5		
4	0: binary, 1: 2-er complement	
..		
1	Test Mode Bit 1	
0	Test Mode Bit 0	

The power up default value is 0x0

Test Mode Bit 1	Test Mode Bit 0	DAC Test Mode
0	0	Data from DAC Data register
0	1	Ramp Test Mode
1	0	ADC1/ADC2 -> DAC1/DAC2
1	1	reserved

Note: ADC 1 Clock is used as DAC clock

7.17 DAC Data register (0x46, read/write)

```
#define SIS8300_DAC_DATA_REG        0x46  /* read/write; D32 */
```

Bit	write
31	DAC2 Data 15
...	
...	
16	DAC2 Data 0
15	DAC1 Data 15
...	
...	
0	DAC1 Data 0

The power up default value is 0x0

7.18 ADC Serial Interface (SPI) interface register (0x48, read/write)

```
#define SIS8300_ADC_SERIAL_INTERFACE_REG       0x48  /* read/write; D32 */
```

Several parameters of the ADC AD9268 chip can be configured with the SPI (serial Peripheral Interface).
Please refer to the documentation of the ADC AD9268 chip for details.

Bit	write	read
31	ADC Synch cmd	Write/Read Logic BUSY Flag
...		
...		
26	ADC Select Mux Bit 2	
25	ADC Select Mux Bit 1	
24	ADC Select Mux Bit 0	
23	Read Cmd	
22		
21		
20	Address Bit 12	
19	Address Bit 11	
12	Address Bit 4	
11	Address Bit 3	
10	Address Bit 2	
9	Address Bit 1	
8	Address Bit 0	
7	Write Data Bit 7 (MSB)	Read Data Bit 7 (MSB)
6	Write Data Bit 6	Read Data Bit 6
..		
1	Write Data Bit 1	Read Data Bit 1
0	Write Data Bit 0 (LSB)	Read Data Bit 0 (LSB)

The power up default value is 0x0

ADC Synch Cmd : generates an synch pulse with AD9510 #1 FPGA clock

7.19 ADC Input Tap delay registers (0x49)

```
#define SIS3305_ADC_INPUT_TAP_DELAY                    0x49
```

The input tap delay registers are used to adjust the FPGA data strobe timing.

Bit	31-13	12	11	10	9	8	7-6	5-0
Function	None	ADC 9/10 Select	ADC 7/8 Select	ADC 5/6 Select	ADC 3/4 Select	ADC 1/2 Select	None	Tap delay value (x 78ps)

Bit	write	read
31		Tap Delay Logic BUSY Flag
...		
..		
..		
12	ADC 9/10 Select Bit	
11	ADC 7/8 Select Bit	
10	ADC 5/6 Select Bit	
9	ADC 3/4 Select Bit	
8	ADC 1/2 Select Bit	
7	Tap delay value Bit 7	Tap delay value Bit 7
6	Tap delay value Bit 6	Tap delay value Bit 6
..		
1	Tap delay value Bit 1	Tap delay value Bit 1
0	Tap delay value Bit 0	Tap delay value Bit 0

7.20 Virtex 5 System Monitor registers

```
#define SIS8300_VIRTEX5_SYSTEM_MONITOR_DATA_REG      0x90
#define SIS8300_VIRTEX5_SYSTEM_MONITOR_ADDR_REG      0x91
#define SIS8300_VIRTEX5_SYSTEM_MONITOR_CTRL_REG      0x92

The Virtex 5 system monitor registers give access to temperature and
voltages of the FPGA on the SIS8300.
```

Refer to the sysmon.c routine and the Virtex 5 FPGA documentation for details.

7.21 Trigger setup register registers

```
#define SIS8300_TRIGGER_SETUP_CH1_REG          0x100  /* rd/wr D32 */
..
#define SIS8300_TRIGGER_SETUP_CH10_REG         0x109  /* rd/wr D32 */
```

These read/write registers hold the 8-bit wide trigger pulse length (in sample clocks), the Peaking and Gap Time of the trapezoidal FIR filter.
(Gap Time = SumG Time – Peaking Time)

Bit	Function	
31	Reserved	
..	..	
26	Enable Trigger	
25	GT trigger condition	
24	FIR Trigger Mode	
23	Puls Length bit 7	Trigger Pulse Length
22	Puls Length bit 6	
21	Puls Length bit 5	
20	Puls Length bit 4	
19	Puls Length bit 3	
18	Puls Length bit 2	
17	Puls Length bit 1	
16	Puls Length bit 0	
15	reserved	SumG time (only FIR trigger) (time between both sums)
14	reserved	
13	reserved	
12	SumG bit 4	
11	SumG bit 3	
10	SumG bit 2	
9	SumG bit 1	
8	SumG bit 0	
7	reserved	Peaking time P (only FIR trigger) $\sum_{i=x}^{x+P} Si$
6	reserved	
5	reserved	
4	P bit 4	
3	P bit 3	
2	P bit 2	
1	P bit 1	
0	P bit 0	

The power up default value reads 0x 00000000

Si: Sum of ADC input sample stream from x to x+P
P: Peaking time (number of values to sum)
SumG: SumGap time (distance in clock ticks of the two running sums)

The maximum SumG time: 16 (clocks)
The minimun SumG time: 1 (clocks)
Values > 16 will be set to 16
Value = 0 will be set to 1

The maximum Peaking time: 16 (clocks)
The minimun Peaking time: 1 (clocks)
Values > 16 will be set to 16
Value = 0 will be set to 1

7.22 Trigger Threshold registers

```
#define SIS8300_TRIGGER_THRESHOLD_CH1_REG            0x110  /* rd/wr D32 */
..
#define SIS8300_TRIGGER_THRESHOLD_CH10_REG           0x119  /* rd/wr D32 */
```

These read/write registers hold the threshold values for the 10 ADC channels.

7.22.1 Trigger Threshold

Bit	31-16	15-0
Function	Threshold value OFF	Threshold value ON

default after Reset: 0x0

A trigger output pulse is generated on two conditions:

- GT is set (GT) in trigger setup register:
  the trigger Out pulse will be issued if the actual sampled ADC value **goes** above the threshold value ON **and** OFF. A new Trigger Out Pulse will be suppressed until the ADC value **goes** below the threshold value OFF.

- GT is cleared (LT) in trigger setup register:
  the trigger Out pulse will be issued if the actual sampled ADC value **goes** below the threshold value ON **and** OFF. A new trigger Out pulse will be suppressed until the ADC value **goes** above the threshold value OFF.

  the trigger Out pulse will be issued if the actual sampled ADC value **goes** below the threshold value.

GT: greater than
LT: lower than

7.22.2 FIR Trigger Threshold

Bit	31-20	19-0
Function	None	**Trapezoidal t**hreshold value

default after Reset: 0x0

The value of the Sum (trapezoidal value) depends on the peaking time P. Therefore the selection of the value of the Trapezoidal threshold depends on P also.

Trapezoidal value calculation:
Trapezoidal value = (SUM2 – SUM1)

Where

$$SUM1 = \sum_{i=x}^{x+P} Si$$

$$SUM2 = \sum_{j=x+sumG}^{x+P+sumG} Sj$$

The FIR filter logic generates the Trapezoidal by subtraction of the two running sums. This implies, that the internal value of the trapezoid is on average 0.

A trigger output pulse is generated:

- GT is set (GT):
  the Trigger Out Pulse will be issued if the actual trapezoidal value **goes** above the programmable trapezoidal threshold value

- GT is cleared (LT):
  the Trigger Out Pulse will be issued if the actual trapezoidal value **goes** below the **negated** programmable trapezoidal threshold value

7.23 Memory Sample Start Address / Actual Sample Address registers

```
#define SIS8300_SAMPLE_START_ADDRESS_CH1_REG   0x120 /* rd/wr D32 */
..
#define SIS8300_SAMPLE_START_ADDRESS_CH10_REG  0x129 /* rd/wr D32 */
```

The write function to these registers defines the memory start address.
The value is given in 256-bit blocks.

ADC ch1 Memory Sample Start Address / Actual Address register

Bit	31-24	23-0
Write Function	reserved	Memory Sample Start Address (256-bit blocks) (16-bit word address x 16)

default after Reset: 0x0

The power up default value is 0

Explanation (memory sample start address)
The contents of the **sample memory start address** register is assigned as memory data storage address with the arm command (key address arm sampling) or with the enable command (key address enable sampling).

The read function from these registers give the information of the actual sampling address for the given ADC channel.
(at the moment: only valid if the logic is not busy!)

The value is given in 256-bit Blocks (16bit word address x 16)

Bit	31-24	23-0
Read Function	reserved	Actual Sample Memory Address (in 256-bit Blocks) (16-bit word address x 16)

the power up default value is 0

7.24 Sample Length register

```
#define SIS8300_SAMPLE_LENGTH_REG        0x12A /* rd/wr D32 */
```

This register defines the number of sample blocks of each ADC Event or.

The size of one sample block for each ADC channel is 256-bit (16 x 16-bit word).

Bit	31-24	7-0
Function	reserved	Sample Block Length

default after Reset: 0x0

7.25 Ringbuffer Pretrigger Delay register

```
#define SIS8300_PRETRIGGER_DELAY_REG                0x12B /* rd/wr D32 */
```

This register defines the number of pre trigger delay samples for all channels.
The maximum pre trigger delay value is 2046.

Bit	31-26	10-0
Function	reserved	Delay value

8 RTM management

Connected RTMs shall be compliant to the PICMG MTCA.4 specification in a way that they must have an on board I²C EEProm (on address 0x50) and a NXP PCF8574-compatible port expander (on address 0x7C).

Required port expander connection map for normal operation:

Port pin	Function
P0	HotSwap Switch (low active)
P1	LED Blue (low active)
P2	LED Red (low active)
P3	LED Green (low active)
P4	PowerGood (low active)
P5	Reset (low active)
P6	PowerEnable (low active)
P7	EEprom Write Protect

The EEprom shall contain any relevant device information (FRU records) about the RTM (refer to PICMG AMC.0). Additionally the EEprom shall contain the new record types defined in PICMG MTCA.4.

In order to be able to decide whether a connected RTM is compatible to the SIS8300 the RTM record shall contain one of the Zone 3 Identifier records listed in the table below.

Supported Zone 3 Identifier Records (Interface Identifier OEM):

IANA PEN (Private enterprise number)	Zone 3 OEM record	Descripton
0x0092BD (37565)	0x83000001	SIS8300 Zone3 - v1 compatibility
0x00053F (1343)	0x08020000	DESY DWC Zone3 compatibility

9 Appendix

9.1 Power Consumption

The currents drawn by the SIS8300 are listed in the table below.

Voltage	Current
3,3 V	100 mA
12 V	2 A

These currents are typical values during normal operation. They can vary depending on the loaded firmware design.

9.2 Ordering options

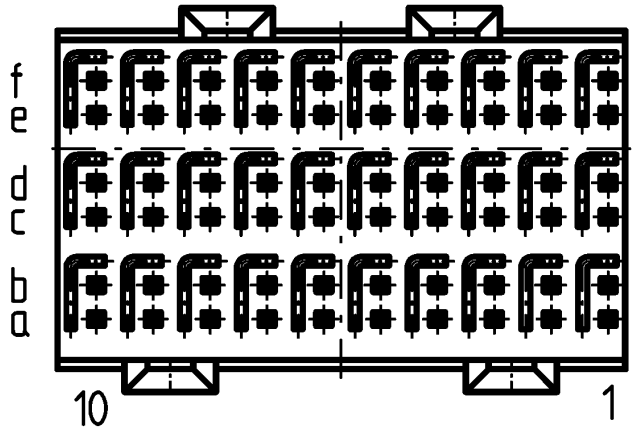
The available part numbers are listed in the table below.

Struck part number	FPGA	Memory
04075	SIS8300 V2 with XC5VLX50T-3FFG1136C	4 x 1 GBit
To be defined	XC5VLX110T-1/3FFG1136C	5 x 1 GBit

Note: The V1 and V2 preseries cards are stuffed with the fastest available speed grade -3. A lower speed grade -1 version may be desirable for high volume applications when speed considerations are not an issue.

9.3 RTM/Zone 3 connectors J75 and J76

J75 and J76 are 90 pin right angle female connectors providing 30 contact pairs each (60 signal contacts and 30 ground contacts). Every contact pair is surrounded by a “L” shaped male shield blade. The shielding contact is designated with the names of the corresponding signal pair (signal pin a and b is affiliated with shielding contact ab e.g.). The picture below shows the connector contact layout as seen from the rear side of the board.



9.3.1 J75 connector pin assignments

The J75 connector routes the differential analog input signals of the ADC channels and ground to the RTM. The characters “TF” in signal names stand for signals to the AC coupled transformer input stages. In same fashion “PA” stands for DC coupled preamplifier input stage.

Col → Row ↓	ef	f	e	cd	d	c	ab	b	a
10	GND	CH9_PA-	CH9_PA+	GND	GND	GND	GND	CH0_TF-	CH0_TF+
9	GND	CH1_TF-	CH1_TF+	GND	GND	GND	GND	CH8_PA-	CH8_PA+
8	GND	CH7_PA-	CH7_PA+	GND	GND	GND	GND	CH2_TF-	CH2_TF+
7	GND	CH3_TF-	CH3_TF+	GND	GND	GND	GND	CH6_PA-	CH6_PA+
6	GND	CH5_PA-	CH5_PA+	GND	GND	GND	GND	CH4_TF-	CH4_TF+
5	GND	CH5_TF-	CH5_TF+	GND	GND	GND	GND	CH4_PA-	CH4_PA+
4	GND	CH3_PA-	CH3_PA+	GND	GND	GND	GND	CH6_TF-	CH6_TF+
3	GND	CH7_TF-	CH7_TF+	GND	GND	GND	GND	CH2_PA-	CH2_PA+
2	GND	CH1_PA-	CH1_PA+	GND	GND	GND	GND	CH8_TF-	CH8_TF+
1	GND	CH9_TF-	CH9_TF+	GND	GND	GND	GND	CH0_PA-	CH0_PA+

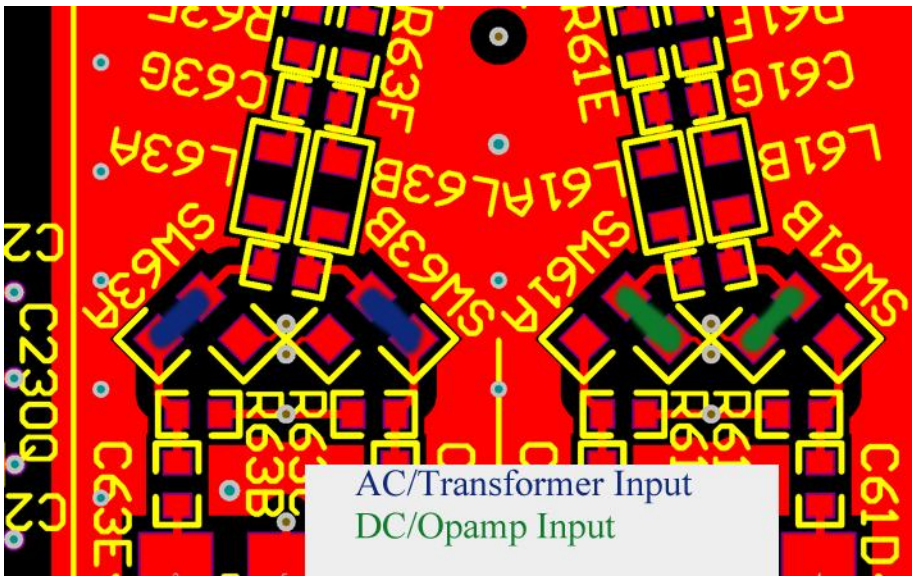
9.3.2 J76 connector pin assignments

The J76 connector is used to route power, data and system management pins to the RTM board.

Col → Row ↓	ef	f	e	Cd	d	c	ab	b	a
10	GND	GND	GND	GND	GND	GND	GND	GND	GND
9	GND	CLK1-	CLK1+	GND	GND	GND	GND	CLK0-	CLK0+
8	GND	GND	GND	GND	CLK2-	CLK2+	GND	GND	GND
7	GND	GND	GND	GND	GND	GND	GND	GND	GND
6	GND	D11-	D11+	GND	D10-	D10+	GND	D9-	D9+
5	GND	D8-	D8+	GND	D7-	D7+	GND	D6-	D6+
4	GND	D5-	D5+	GND	D4-	D4+	GND	D3-	D3+
3	GND	D2-	D2+	GND	D1-	D1+	GND	D0-	D0+
2	GND	SCL_I	SCL_E	GND	SCL	MP+3.3V	GND	PWR+12V	PWR+12V
1	GND	SDA_I	SDA_E	GND	SDA	PS#	GND	PWR+12V	PWR+12V

9.3.3 Note on AC/DC input stage selection

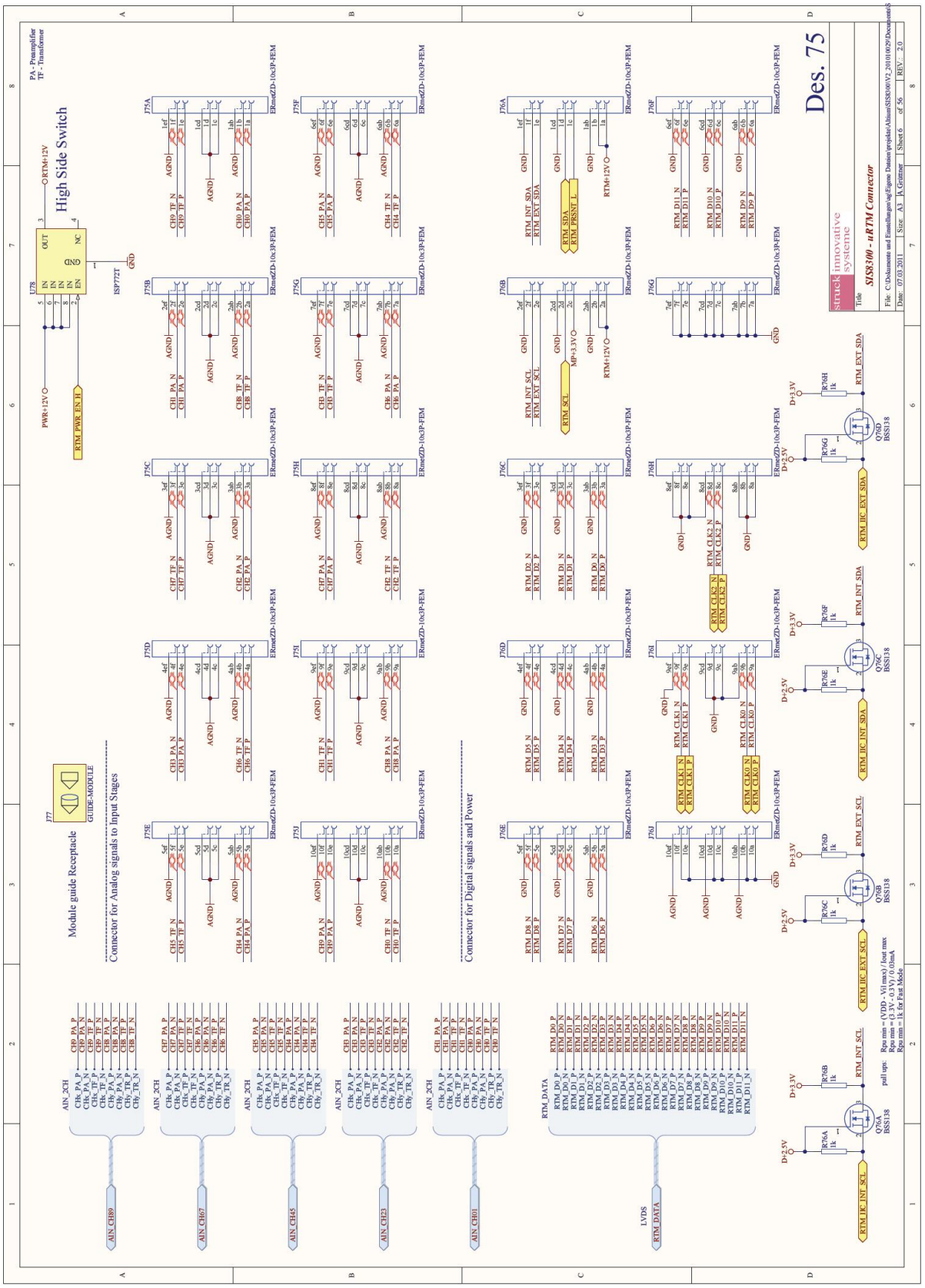
The AC (transformer) or DC (operation amplifier Opamp) input path is selected on the SIS8300 card via 0603 solder bridges as illustrated for channels 0 and 1 on the screenshot below. The designators for all channels can be found in the table below.



xxx

ADC Channel	Designator	Input for ADC
0	SW63A	ADC_CH0+
0	SW63B	ADC_CH0-
1	SW61A	ADC_CH1+
1	SW61B	ADC_CH1-
2	SW58A	ADC_CH2+
2	SW58B	ADC_CH2-
3	SW56A	ADC_CH3+
3	SW56B	ADC_CH3-
4	SW53A	ADC_CH4+
4	SW53B	ADC_CH4-
5	SW51A	ADC_CH5+
5	SW51B	ADC_CH5-
6	SW48A	ADC_CH6+
6	SW48B	ADC_CH6-
7	SW46A	ADC_CH7+
7	SW46B	ADC_CH7-
8	SW43A	ADC_CH8+
8	SW43B	ADC_CH8-
9	SW41A	ADC_CH9+
9	SW41B	ADC_CH9-

9.4 RTM connector schematics



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